Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A computer system, comprising:
   a central processing unit (CPU);
   a bridge coupled to the CPU for providing a bus;
   a first slot configured to receive a device, wherein a first ~~portion~~ set of lanes of the ~~bridge~~ bus is coupled to the first slot;
   a second slot configured to receive a device, wherein a second ~~portion~~ and different set of lanes of the ~~bridge~~ bus is coupled to the second slot;
   at least one trace coupled to the first and second slots; ~~and~~
   ~~whereby~~ wherein the computer system is configured so that inserting a jumper board in the first slot couples the first ~~portion~~ set of lanes of the ~~bridge~~ bus to the second slot via the at least one trace, while the jumper board does not occupy the second slot; and
   wherein the slots are implemented together on a board other than the jumper board.

2. (Canceled)

3. (Currently amended) The computer system of claim 1, wherein each slot is capable of providing all signals pertaining to [[a]] the bus.

4. (Currently amended) A computer system, comprising:
   a central processing unit (CPU);
   a bridge coupled to the CPU for providing a bus;
   a first slot configured to receive a device, wherein a first ~~portion~~ set of lanes of the ~~bridge~~ bus is coupled to the first slot;

a second slot configured to receive a device, wherein a second ~~portion~~ and different set of lanes of the ~~bridge~~ bus is coupled to the second slot;

at least one trace coupled to the first and second slots; and

a jumper board;

~~whereby~~ wherein the computer system is configured so that inserting [[a]] the jumper board in the first slot couples the first ~~portion~~ set of lanes of the ~~bridge~~ bus to the second slot, wherein the slots are implemented on a riser board.

5. (Original) The computer system of claim 4, wherein lane polarity inversion techniques are implemented on a printed circuit board that includes the first and second slots.

6. (Original) The computer system of claim 4, wherein lane reversal techniques are implemented on a printed circuit board that includes the first and second slots.

7. (Currently amended) A computer system, comprising:

a central processing unit (CPU);

a bridge coupled to the CPU for providing a bus;

a first slot configured to receive a device, wherein a first ~~portion~~ set of lanes of the ~~bridge~~ bus is coupled to the first slot;

a second slot configured to receive a device, wherein a second ~~portion~~ and different set of lanes of the ~~bridge~~ bus is coupled to the second slot;

at least one trace coupled to the first and second slots; ~~and~~

~~whereby~~ wherein the computer system is configured so that inserting a jumper board in the first slot couples the first ~~portion~~ set of lanes of the ~~bridge~~ bus to the second slot, wherein the first and second ~~portions~~ sets of lanes of the ~~bridge include~~ bus each form a serial bus; and

wherein the slots are implemented together on a board other than the jumper board.

8. (Original) The computer system of claim 7, wherein the serial bus comprises an optical bus.

9. (Original) The computer system of claim 7, wherein the serial bus is a PCI-Express bus.

10. (Original) The computer system of claim 7, wherein the slots do not provide connections for all signals pertaining to the bus without the jumper board.

11. (Currently amended) A method of providing a bus in a computer system, comprising:

routing a first portion of the bus to a first segment of a first slot;

routing a second and different portion of the bus to a first segment of a second slot;

coupling a second segment of the first slot via at least one trace to a second segment of the second slot; and

inserting a jumper board into the first slot;

wherein the slots are implemented together on a board other than the jumper board; and

wherein the jumper board connects the first and second segments of the first slot, thereby routing the first portion of the bus to the second slot via the at least one trace, while the jumper board does not occupy the second slot.

12. (Original) The method of claim 11, wherein the first and second portions of the bus comprise the entire bus.

13. (Currently amended) The method of claim 11, further comprising selecting the first and second slots, from among several available slot configurations, to correspond to a maximum number of physical ~~lines~~ lanes of the bus.

14. (Previously amended) The method of claim 11, further comprising adjusting the first and second slots such that they can physically accommodate more than just the first and second portions.

15. (Original) The method of claim 14, wherein the first and second slots are capable of providing all signals that pertain to the entire bus.

16. (Original) The method of claim 11, wherein the connection between slots occurs on a system board.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)